UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,078	11/25/2003	Ki-Ju Lee	1793.1087	4901

21171 7590 04/20/2006

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DOGAN, ERIN L	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,078	LEE, KI-JU	
	Examiner	Art Unit	
	Erin L. Dogan	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-21 and 23-39* is/are rejected.

7)☒ Claim(s) *7 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/05, 11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are being pending in the application.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 8, 9, 14-17, 23-24, 29-31, 38 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Chaiken et al et al (US6,757,838,B1).

3. For Claim 1, Chaiken et al discloses a flash memory, comprising: a first boot zone storing a first booting program; a second boot zone storing a duplicate of the first booting program, as a second booting program; and a data zone storing an executable firmware program, wherein one of the first and second booting programs is executed based on whether an error is detected in either of the first or second boot zones (Column 2, lines 43-50).

4. For Claim 2, Chaiken et al discloses a memory protection apparatus, of an AT Attachment Packet Interface (ATAPI) drive for storing an executable firmware program, downloaded from a host, the apparatus comprising: a storage unit having a first boot zone storing a first booting program, a second boot zone storing a duplicate of the first booting program, as a second booting program, and a data zone storing the firmware program; and a controller checking for a presence of an error in the first and/or second booting zones when the ATAPI drive is initialized, executing one of the first booting

program and the second booting program based on whether the first or second boot zones include an error, and controlling execution of the firmware program (Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces.], Column 2, lines 43-67).

5. For Claims 8, 14, 16, 23, and 29, Chaiken et al discloses an apparatus, method and a memory wherein the host is a computer and the ATAPI drive and the computer communicate using an ATAPI protocol l(Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces], Figure 1).

6. For Claim 9, Chaiken et al discloses a method of operating an ATAPI drive for storing an executable firmware program downloaded from a host, the method comprising: detecting for an error in a first boot zone of a memory, storing a first booting program, and a second boot zone of the memory, storing a duplicate of the first booting program, as a second booting program, when the ATAPI drive is initialized; executing one of the first and second booting programs based on whether the first boot zone or the second boot zone includes an error; and accessing the data zone of the memory in which the firmware program is stored and executing the firmware program after the executed one booting program (Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces], Column 2, lines 43-58, Figure 1 and 4, Column 6, lines 31-34, 49-52).

7. For Claim 15, Chaiken et al discloses a flash memory, comprising: a first memory having a first boot zone storing a first booting program and a second boot zone storing a duplicate of the first booting program, as a second booting program; and a second memory having a data zone storing an executable downloaded firmware program, wherein one of the first and second booting programs is executed based on an error being detected in the first boot zone or the second boot zone (Column 2, lines 43-50, Column 6, lines 31-34, 49-52, Column 1, lines 14-38).

8. For Claim 17, Chaiken et al discloses A memory protection apparatus, including an ATAPI drive for storing an executable firmware program downloaded from a host, the apparatus comprising: a first storage unit having a first boot zone storing a first booting program and a second boot zone storing a duplicate of the first booting program, as a second booting program; a second storage unit storing the firmware program; and a controller detecting for an error in one of the first and second boot zones when the ATAPI drive is initialized, executing the first booting program or the second booting program based on whether the one boot zone is the first boot zone or the second boot zone, and controlling execution of the firmware program stored in the data zone of the second storage unit (Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces], Column 2, lines 43-58, Figure 1 and 4, Column 6, lines 31-34, 49-52, Column 1, lines 14-38).

9. For Claim 24, Chaiken discloses a method of operating an ATAPI drive, storing an executable firmware program downloaded from a host, the method comprising: detecting for an error in first and second boot zones of a first storage unit when the ATAPI drive is initialized, the first boot zone storing a first booting program and the second boot zone storing a duplicate of the first booting program, as a second booting program; executing one of the first and second booting programs based on whether the corresponding first or second boot zone has no error; and accessing a data zone of a second storage unit, storing the firmware program, and executing the firmware program after the execution of the one booting program (Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces], Column 2, lines 43-58, Figure 4, Column 6, lines 31-34, 49-52, Column 1, lines 14-38).

10. For Claim 30, Chaiken discloses a storage system, comprising: a first memory storing more than one booting program; a second memory storing a firmware program for the storage system, separately addressable from the first memory; and a controller checking for a presence of an error in a first memory portion, of the first memory, when a storage drive containing the first memory is initialized, executing a first booting program, stored in the first memory portion, if no error is detected in the first memory portion, and executing a different booting program stored in a different memory portion of the first memory, if the error is detected in the first memory portion, and executing the firmware program after executing a booting program (Column 4, lines 38-43 [An ATAPI

drive is a drive that uses IDE interfaces], Column 2, lines 43-58, Figure 4, Column 6, lines 31-34, 49-52, Column 1, lines 14-38).

11. For Claim 31, Chaiken et al discloses a storage system wherein the first memory is divided into separately addressable memory portions, including the first memory portion, with at least two memory portions including booting programs (Column 3, lines 5-13).

12. For Claim 38, Chaiken disclose a storage system further comprising a host communicating to the second memory to store the firmware in the second memory (Column 1, lines 14-38).

13. For Claim 39, Chaiken et al discloses a storage system wherein the first and second memories are in an AT Attachment Packet Interface (ATAPI) drive and the host is a computer communicating with the ATAPI drive using an ATAPI protocol (Column 4, lines 38-43 [An ATAPI drive is a drive that uses IDE interfaces]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3-6, 10-13,18-21,25-28,32-33,34-37, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaiken et al (US 6,757,838 B1) as applied to claims 1-2, 9, 15, 17, 24 and 30 above, and further in view of Lin (US 6,892,323 B2).

15. For Claims 3, 10, 18, 25 and 32, Lin discloses an apparatus, method and a system wherein the controller detects and corrects for an error in the second boot zone while executing the first booting program, when no error is detected in the first boot zone (Column 8, lines 10-16).

16. For Claims 4, 11, 19, 26, and 33, Lin discloses an apparatus, method and a system wherein data stored in the first boot zone, which has no error, is used as a basis for the detection and correction of the error in the second boot zone (Column 8, lines 10-16).

17. For Claims 5, 12, 20, 27, and 35, Lin discloses an apparatus, method and a system wherein the controller corrects for an error in the first boot zone while executing the second booting program, when the error is detected in the first boot zone (Column 8, lines 35-39).

18. For Claims 6, 13, 21, 28, and 36, Lin discloses an apparatus, method and a system wherein data in the second boot zone, which has no error, is used as a basis for the correction of the error in the first boot zone (Column 8, lines 35-39).

19. For Claim 34, Lin discloses a storage system wherein a booting program of the second memory portion is replaced by the first booting program during the correction of the error in the second memory portion (Column 8, lines 10-16).

20. For Claim 37, Lin discloses a storage system wherein the first booting program of the first memory portion is replaced by the second booting program during the correction of the error in the first memory portion (Column 8, lines 35-39).

21. Chaiken et al, however does not teach of an apparatus, method or system wherein the corrupted boot zone area can be replaced by another boot zone that contains no errors. Specifically, Chaiken et al teaches of checking a designated/primary boot zone area for errors. If errors are found, switching to a second boot zone/backup boot area to allow continuation of the booting process.

22. It would have been obvious to one of ordinary skill in the art to combine the teachings of Chaiken and Lin because they both teach methods for the continuation of the booting process when incurring an error, by switching to a second/backup copy of the corrupted boot zone. Lin teaches of an apparatus, method or system wherein the

corrupted boot zone area can be replaced by another boot zone that contains no errors. This provides the ability to recover the corrupted bios and allow there to always to be a good version of the bios to be available to switch to if needed.

Allowable Subject Matter

23. Claims 7 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin L. Dogan whose telephone number is 571-272-1412. The examiner can normally be reached on Mon-Fri 8:00-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin Dogan
Patent Examiner
Art Unit 2115

CHUN CAO
PRIMARY EXAMINER